ECT312	DIGITAL SYSTEM DESIGN	CATEGORY	L	T	P	CREDIT
		PEC	2	1	0	3

Preamble: This course aims to design hazard free synchronous and asynchronous sequential circuits and implement the same in the appropriate hardware device

Prerequisite: ECT203 Logic Circuit Design

Course Outcomes: After the completion of the course the student will be able to

CO 1 K4	Analyze clocked synchronous sequential circuits
CO 2 K4	Analyze asynchronous sequential circuits
CO 3 K3	Design hazard free circuits
CO 4 K3	Diagnose faults in digital circuits
CO 5 K2	Summarize the architecture of FPGA and CPLDs

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO1	3	3	3		2				2	2		3
CO2	3	3			2				2	2		3
CO3	3	3	3	3					2	2		3
CO4	3	2		1					2	2		3
CO5	2								2	2		3

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination
	1	2	
Remember K1	10	10	15
Understand K2	10	20	30
Apply K3	20	20	35
Analyse K4	10		20
Evaluate			
Create			

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance : 10 marks

Continuous Assessment Test (2 numbers) : 25 marks

Assignment/Quiz/Course project : 15 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

Course Level Assessment Questions

Course Outcome 1 (CO1): Analyze clocked synchronous sequential circuits (K4)

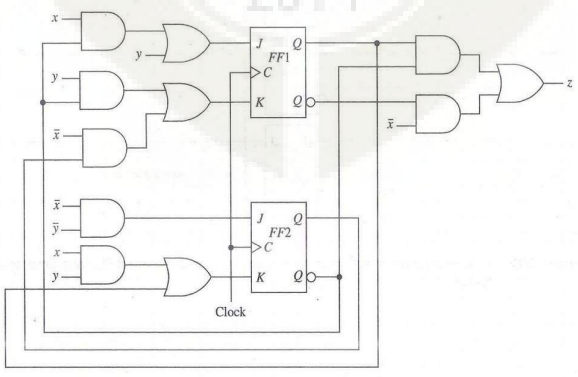
1. Construct an ASM chart for a sequence recognizer to recognize the input sequence of pairs x1x2= 01, 01, 11, 00. The output variable, 'z' is asserted when x1x2= 00 if and only if the three preceding pairs of inputs are x1x2= 01, 01 and 11, in that order.

2. Obtain a minimal state table for a clocked synchronous sequential network having a single input line 'x' in which the symbols 0 and 1 are applied and a single output line 'z'. An outputof 1 is to be produced if and only if the 3 input symbols following two consecutive input 0's consist of at least one 1. An example of input/output sequences that satisfy the conditions of the network specifications is:

   x=0100010010010010000000011

   z=0000001000000100000000001

3. Analyse the following clocked synchronous sequential network. Derive the next state and output equations. Obtain the excitation table, transition table, state table and state diagram.

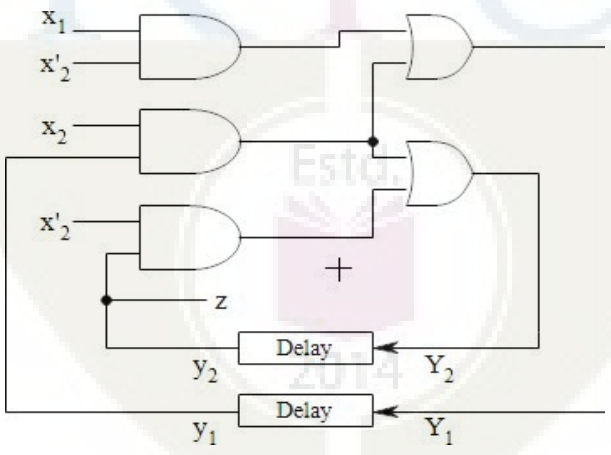


Course Outcome 2 (CO2): Analyze asynchronous sequential circuits (K4)

1. A reduced flow table for a fundamental-mode asynchronous sequential network is given below. Using the universal multiple-row state assignment, construct the corresponding expanded flow table and transition table. Assign outputs where necessary such that there is at most a single output change during the time the network is unstable. Assume that the inputs x1 and x2 never change simultaneously.

Present state	Next state				Output (z)			
	Input state (x_1x_2)				Input state (x_1x_2)			
	00	01	10	11	00	01	10	11
A	(A)	B	(A)	D	1	-	0	-
B	D	(B)	(B)	C	-	0	1	-
C	A	(C)	(C)	(C)	-	1	1	0
D	(D)	C	A	(D)	0	-	-	1

2. Analyze the asynchronous sequential network by forming the excitation/transition table, state table, flow table and flow diagram. The network operates in the fundamental mode with the restriction that only one input variable can change at a time.



3. Describe races in ASN with example.

Course Outcome 3 (CO3): Design hazard free circuits (K3)

1. Differentiate between static and dynamic hazard.
2. Examine the possibility of hazards in the (i) OR-AND logic circuit whose Boolean function is given by $f = \sum(0,2,6,7)$ (ii) AND-OR logic circuit whose Boolean function is given by $f = \sum(3,4,5,7)$. Show how the hazard can be detected and eliminated in each circuit.

3. Investigate the problem of clock skew in practical sequential circuits and suggest solutions with justification to minimize or eliminate it.

Course Outcome 4 (CO4): Diagnose faults in digital circuits (K3)

1. Illustrate the fault table method used for effective test set generation for the circuit whose Boolean function is $z = \overline{x_1}x_2 + x_3$
2. Find the test vectors of all SA0 and SA1 faults of the circuit whose Boolean function is $f = \bar{x}_1 x_2 + x_1 x_2 x_3$ by the Kohavi algorithm.
3. Write a note on BIST techniques.

Course Outcome 5 (CO5): Summarize the architecture of FPGA and CPLDs (K2)

1. Draw and explain the architecture of Xilinx XC4000 configurable logic block.
2. Draw and explain the architecture of Xilinx 9500 CPLD family.
3. Explain the internal structure of XC4000 input/output block.

SYLLABUS

Module 1: Clocked Synchronous Networks

Analysis of clocked Synchronous Sequential Networks (CSSN), Modelling of CSSN – State assignment and reduction, Design of CSSN, ASM Chart and its realization

Module 2: Asynchronous Sequential Circuits

Analysis of Asynchronous Sequential Circuits (ASC), Flow table reduction- Races in ASC, State assignment problem and the transition table- Design of AS, Design of ALU

Module 3: Hazards

Hazards – static and dynamic hazards – essential, Design of Hazard free circuits – Data synchronizers, Mixed operating mode asynchronous circuits, Practical issues- clock skew and jitter, Synchronous and asynchronous inputs – switch bouncing

Module 4: Faults

Fault table method – path sensitization method – Boolean difference method, Kohavi algorithm, Automatic test pattern generation – Built in Self Test (BIST)

Module 5: CPLDs and FPGA

CPLDs and FPGAs - Xilinx XC 9500 CPLD family, functional block diagram– input output block architecture - switch matrix, FPGAs – Xilinx XC 4000 FPGA family – configurable logic block - input output block, Programmable interconnect

Text Books

1. Donald G Givone, Digital Principles & Design, Tata McGraw Hill, 2003
2. John F Wakerly, Digital Design, Pearson Education, Delhi 2002
3. John M Yarbrough, Digital Logic Applications and Design, Thomson Learning

Reference Books

1. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, Digital Systems Testing and Testable Design, John Wiley & Sons Inc.
2. Morris Mano, M.D.Ciletti, Digital Design, 5th Edition, PHI.
3. N. N. Biswas, Logic Design Theory, PHI
4. Richard E. Haskell, Darrin M. Hanna , Introduction to Digital Design Using Digilent FPGA Boards, LBE Books- LLC
5. Samuel C. Lee, Digital Circuits and Logic Design, PHI
6. Z. Kohavi, Switching and Finite Automata Theory, 2nd ed., 2001, TMH

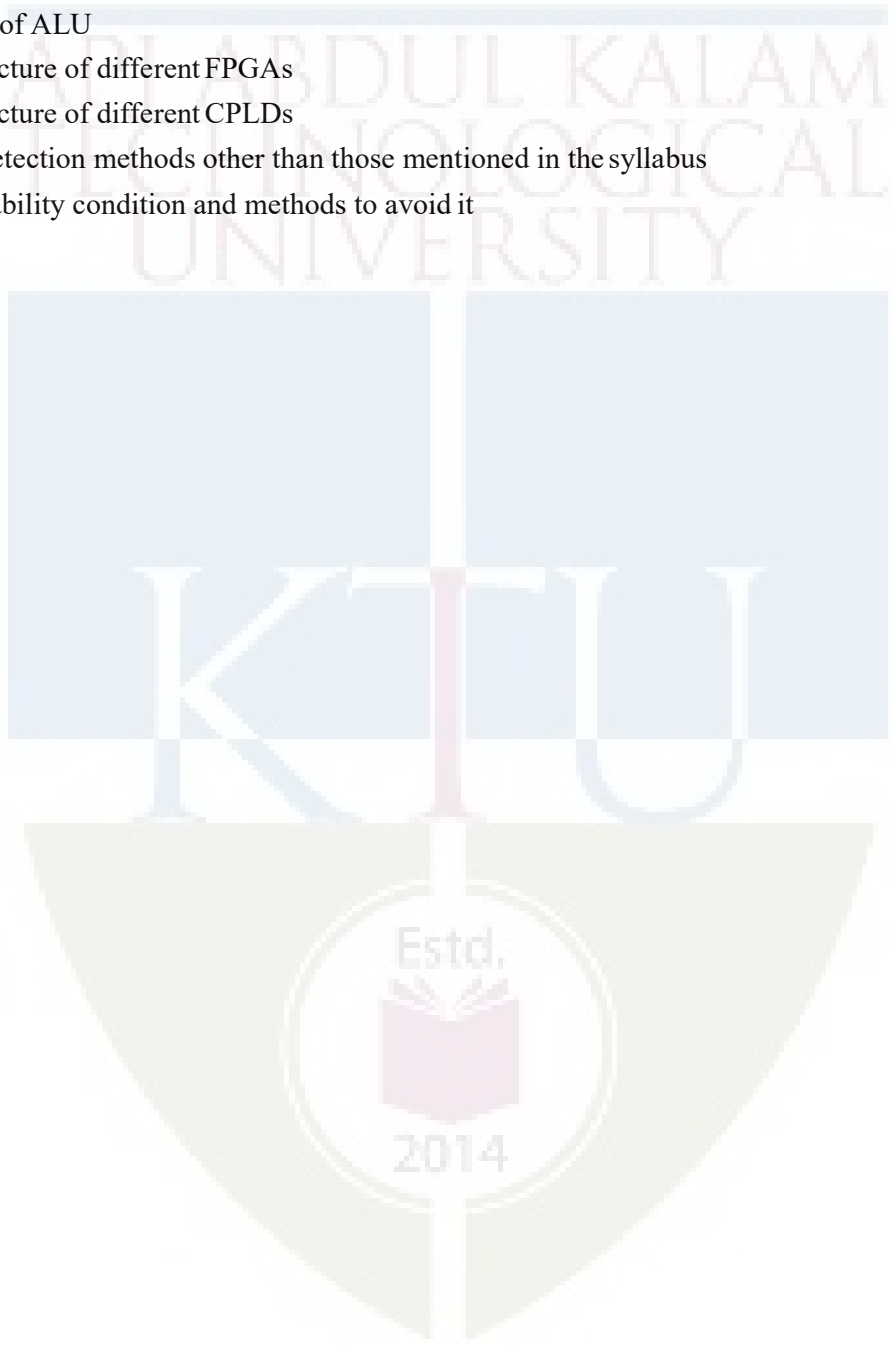
Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**Clocked Synchronous Networks**	
1.1	Analysis of clocked Synchronous Sequential Networks(CSSN)	2
1.2	Modelling of CSSN – State assignment and reduction	2
1.3	Design of CSSN	2
1.4	ASM Chart and its realization	1
2	**Asynchronous Sequential Circuits**	
2.1	Analysis of Asynchronous Sequential Circuits (ASC)	2
2.2	Flow table reduction- Races in ASC	2
2.3	State assignment problem and the transition table- Design of AS	2
2.4	Design of ALU	2
3	**Hazards**	
3.1	Hazards – static and dynamic hazards – essential	1
3.2	Design of Hazard free circuits – Data synchronizers	1
3.3	Mixed operating mode asynchronous circuits	1
3.4	Practical issues- clock skew and jitter	1
3.5	Synchronous and asynchronous inputs – switch bouncing	2
4	**Faults**	
4.1	Fault table method – path sensitization method – Boolean difference method	2
4.2	Kohavi algorithm	2
4.3	Automatic test pattern generation – Built in Self Test(BIST)	3
5	**CPLDs and FPGA**	
5.1	CPLDs and FPGAs - Xilinx XC 9500 CPLD family, functional block diagram– input output block architecture - switch matrix	3
5.2	FPGAs – Xilinx XC 4000 FPGA family – configurable logic block - input output block, Programmable interconnect	3

Simulation Assignments:

At least one assignment should be design of digital circuits that can be used in day today life. This has to be done in a phased manner. The first phase involves the design in HDL (VHDL/ Verilog) and the second phase implementing the same in a hardware device. Some of the assignments are as listed below:

1. Design of vending machine
2. Design of ALU
3. Architecture of different FPGAs
4. Architecture of different CPLDs
5. Fault detection methods other than those mentioned in the syllabus
6. Metastability condition and methods to avoid it



Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SIXTH SEMESTER B.TECH DEGREE EXAMINATION, (**Model Question Paper)**

Course Code: ECT312

Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer ALL Questions. Each carries 3 marks.

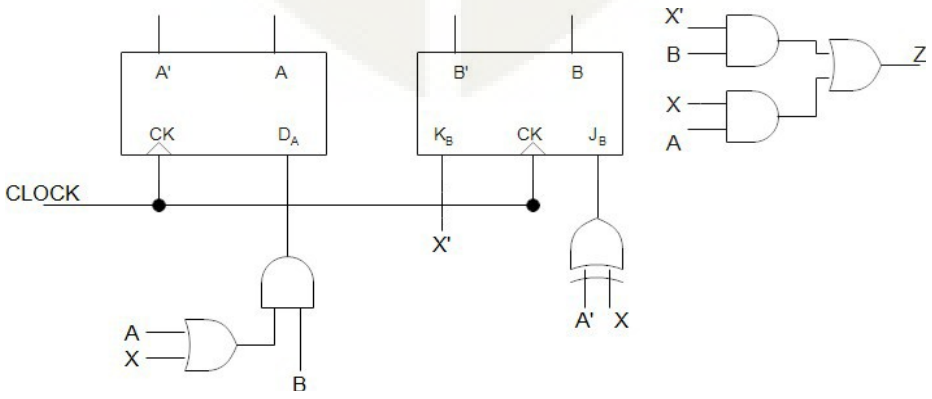
1	Differentiate Mealy and Moore models.	K1
2	What are the elements in an ASM chart?	K1
3	Describe one-hot assignment technique.	K2
4	Define critical and non-critical races.	K1
5	What is jitter? List the sources of clock jitter.	K2
6	Differentiate positive skew and negative skew.	K2
7	List the different types of faults in digital circuits.	K1
8	Differentiate between fault and defect.	K2
9	What are FPGA? What are the advantages of FPGA?	K1
10	Differentiate between FPGA and CPLD	K2

PART – B

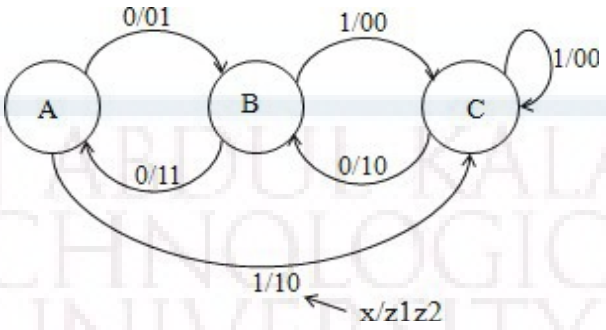
Answer one question from each module; each question carries 14 marks.

Module - I

11 a	Analyze the following sequential network. Derive the next state and output equations. Obtain its transition table and state table.	8	CO1 K4

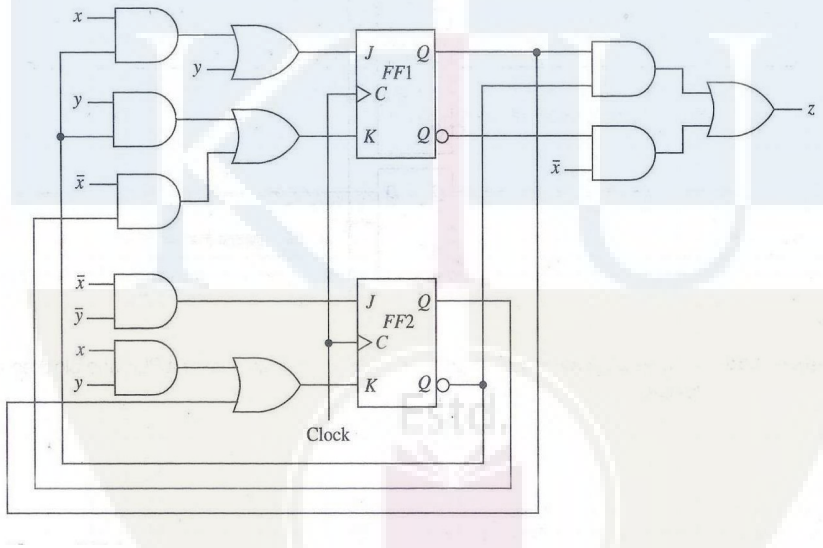


b. Construct an ASM chart for the following state diagram shown. Determine the model of CSSN that this system conforms to with proper justification. 6 CO1 K3



OR

12 For the clocked synchronous sequential network, construct the excitation table, transition table, state table and state diagram. 8 CO1 K4



b. Obtain a minimal state table for a clocked synchronous sequential network having a single input line 'x' in which the symbols 0 and 1 are applied and a single output line 'z'. An output of 1 is to be produced if and only if the 3 input symbols following two consecutive input 0's consist of at least one 1. An example of input/output sequences that satisfy the conditions of the network specifications is: 6 CO1 K3

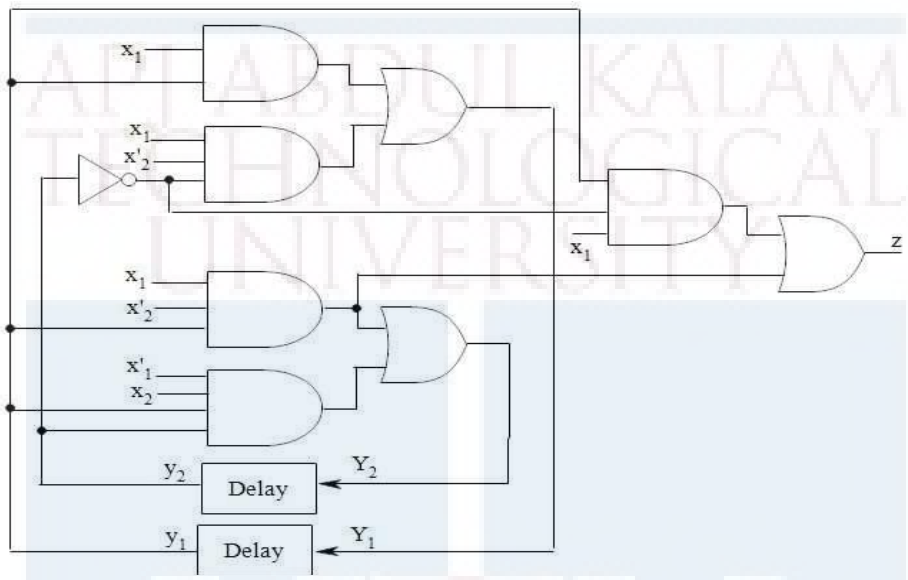
x= 0100010010010010000000011

z= 0000001000000100000000001

Module - II

13a Analyze the asynchronous sequential network by forming the excitation/transition table, state table, flow table and flow diagram. The network operates in the fundamental mode with the restriction that only one input variable can change at a time. 14

CO2
K4



OR

14a A reduced flow table for a fundamental-mode asynchronous sequential network is given below. Using the universal multiple-row state assignment, construct the corresponding expanded flow table and transition table. Assign outputs where necessary such that there is at most a single output change during the time the network is unstable. Assume that the inputs and never change simultaneously. 14

CO2
K4

Present state	Next state				Output (z)			
	Input state (x_1x_2)				Input state (x_1x_2)			
	00	01	10	11	00	01	10	11
A	(A)	B	(A)	D	1	-	0	-
B	D	(B)	(B)	C	-	0	1	-
C	A	(C)	(C)	(C)	-	1	1	0
D	(D)	C	A	(D)	0	-	-	1

Module - III

15a.	Examine the possibility of hazard in the OR-AND logic circuit whose Boolean function is given by $f = \sum(0,2,6,7)$. Show how the hazard can be detected and eliminated.	8	CO3
b.	Explain essential hazards in asynchronous sequential networks. What are the constraints to be satisfied to avoid essential hazards?	6	K3

OR

16a	Draw the logic diagram of the POS expression Y= (x1+x2') (x2+x3). Show that there is a static-0 hazard when x1 and x3 are equal to 0 and x2 goes from 0 to 1. Find a way to remove the hazard by adding one or more gates.	9	CO3 K3
b	Discuss the concept of switch bouncing and suggest a suitable solution.	5	K3

Module - IV

17a	Illustrate the fault table method used for effective test set generation for the circuit whose Boolean function is $z = \overline{x_1}x_2 + x_3$	8	CO 4 K3
b	How can the timing problems in asynchronous sequential circuits be solved using mixed operating mode circuits?	6	K3

OR

18 a.	Find the test vectors of all SA0 and SA1 faults of the circuit whose Boolean function is $f = \bar{x}_1 x_2 + x_1 x_2 x_3$ by the Kohavi algorithm.	8	CO4 K3
b.	Identify different test pattern generation for BIST	6	CO4 K3

Module - V

19	Explain the architecture of XC 4000 FPGA family.	14	CO5 K2

OR

20	Draw and explain the architecture of Xilinx 9500 CPLD family. Also explain the function block architecture.	14	CO5 K2