ECT308	COMPREHENSIVE COURSE WORK	CATEGORY	L	T	P	CREDIT
		PCC	1	0	0	1

Preamble: The objective of this Course work is to ensure the comprehensive knowledge of each student in the most fundamental Program core courses in the curriculum. Five core courses credited from Semesters 3, 4 and 5 are chosen for the detailed study in this course work. This course has an End Semester Objective Test conducted by the University for 50 marks. One hour is assigned per week for this course for conducting mock tests of objective nature in all the listed five courses.

Prerequisite:

1. **ECT202 Analog Circuits**
2. **ECT203 Logic Circuit Design**
3. **ECT301 Linear Integrated Circuits**
4. **ECT303 Digital Signal processing**
5. **ECT305 Analog and Digital communication**

Course Outcomes: After the completion of the course the student will be able to

CO 1	Apply the knowledge of circuit theorems and solid state physics to solve the problems in electronic Circuits
CO 2	Design a logic circuit for a specific application
CO 3	Design linear IC circuits for linear and non-linear circuit applications.
CO 4	Explain basic signal processing operations and Filter designs
CO 5	Explain existent analog and digital communication systems

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	3	1									2
CO 2	3	3	1									2
CO 3	3	3	1									2
CO 4	3	2										2
CO 5	3	2	1									2

Assessment Pattern

Bloom's Category	End Semester Examination
Remember	10
Understand	20
Apply	20
Analyse	
Evaluate	
Create	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
50	0	50	1 hour

End Semester Examination Pattern: Objective Questions with multiple choice (Four). Question paper include Fifty Questions of One mark each covering the five identified courses.

Syllabus

Full Syllabus of all five selected courses

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Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**Analog Circuits**	
1.1	Mock Test on Module 1 and Module 2	1
1.2	Mock Test on Module 3, Module 4 and Module 5	1
1.3	Feedback and Remedial	1
2	**Logic Circuit design**	
2.1	Mock Test on Module 1, Module 2 and Module 3	1
2.2	Mock Test on Module 4 and Module 5	1
2.3	Feedback and Remedial	1
3	**Linear IC**	
3.1	Mock Test on Module 1 and Module 2	1
3.2	Mock Test on Module 3, Module 4 and Module 5	1
3.3	Feedback and Remedial	1
4	**Digital Signal Processing**	
4.1	Mock Test on Module 1, Module 2 and Module 3	1
4.2	Mock Test on Module 4 and Module 5	1
4.3	Mock Test on Module 1, Module 2 and Module 3	1
5	**Analog and Digital Communication**	
5.1	Mock Test on Module 1, Module 2 and Module 3	1
5.2	Mock Test on Module 4 and Module 5	1
5.3	Feedback and Remedial	1