ECT304	VLSI CIRCUIT DESIGN	CATEGORY	L	T	P	CREDIT
		PCC	3	1	0	4

Preamble: This course aims to impart the knowledge of VLSI design methodologies and Digital VLSI circuit design.

Prerequisite:

1. ECT201 Solid State Devices
2. ECT202 Analog Circuits
3. ECT 203 Logic Circuit Design.

COURSE OUTCOMES.

After the completion of the course the student will be able to:

CO1	Explain the various methodologies in ASIC and FPGA design.
CO2	Design VLSI Logic circuits with various MOSFET logic families.
CO3	Compare different types of memory elements.
CO4	Design and analyse data path elements such as Adders and multipliers.
CO5	Explain MOSFET fabrication techniques and layout design rules.

Mapping of course outcomes with program outcomes:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3		3									2
CO2	3	2	3									2
CO3	3	2	3									2
CO4	3	2	3									2
CO5	3		2									2

Assessment Pattern:

Bloom's Category	Continuous Assessment Tests		End Semester Examination
	1	2	
Remember	10	10	20
Understand	20	20	40
Apply	20	20	40
Analyze			
Evaluate			
Create			

Mark distribution:

Total Marks	CIE	ESE	Duration
150	50	100	3Hrs

Continuous Internal Evaluation Pattern:

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignments : 15 marks.

End Semester Examination Pattern

Maximum Marks : 100 **Time : 3 hours**

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks. Mark patterns are as per the syllabus with 75% for theory and 25% for logical/numerical problems.

Course Level Assessment Questions.

CO1:
1. Differentiate between full custom and semi-custom ASIC.
2. With a neat flow chart, explain ASIC design flow.
3. Describe Gate array based ASIC with neat diagram.
4. What are the processes involved in Soc design.

CO2:
1. With a neat diagram explain static and transient analysis of CMOS inverter
2. Realize the given logic function using static CMOS logic and transmission gate logic.
3. Compare the advantages and disadvantages of static and dynamic circuits.

CO3:

1. Compare different ROM structures.
2. Compare static and dynamic RAM structures.
3. Compare the advantages of three transistor and one transistor DRAM cell.

CO4:
1. Design a full adder with static CMOS logic
2. Compare the delay of Carry-Bypass adder, Linear Carry- Select adder, Square- root carry-select adder.

CO5:

1. Explain how electronic grade silicon (EGS) is developed .
2. Explain the necessity of single crystalline silicon in VLSI fabrication and how single crystal silicon is made.
3. Explain diffusion and ion implantation techniques.
4. Explain the advantages of SiO2 and the oxidation techniques.

Syllabus

Module 1: VLSI Design Methodologies.

Introduction: Moore's law .ASIC design, Full custom ASICs, Standard cell based ASICs, Gate array based ASICs, SoCs, FPGA devices, ASIC and FPGA Design flows, Top-Down and Bottom-Up design methodologies. Logical and Physical design. Speed power and area considerations in VLSI design

Module 2: Static CMOS Logic Design

MOSFET Logic Design - NMOS Inverter (Static analysis only), basic logic gates,
CMOS logic, Static and transient analysis of CMOS inverter, Switching power dissipation and delays. Realization of logic functions with static CMOS logic, Pass transistor logic, and transmission gate logic

Module 3: Dynamic logic Design and Storage Cells

Dynamic Logic Design-Pre charge- Evaluate logic, Domino Logic, NP domino logic.
Read Only Memory-4x4 MOS ROM Cell Arrays(OR,NOR,NAND)
Random Access Memory –SRAM-Six transistor CMOS SRAM cell, DRAM –Three transistor and One transistor Dynamic Memory Cell.

Module 4: Arithmetic circuits

Adders: Static adder, Carry-Bypass adder, Linear Carry- Select adder, Square- root carry- select adder. **Multipliers:** Array multiplier.

Module 5: Fabrication techniques and MOSFET physical Design

Material Preparation

Purification and Crystal growth (CZ process), wafer preparation
Thermal Oxidation- Growth mechanisms, Dry and Wet oxidation.
Diffusion and ion implantation techniques.
Epitaxy : molecular beam epitaxy.
Lithography- Photo lithographic sequence, Electron Beam Lithography, Etching and metal deposition techniques.

MOSFET Fabrication techniques

Twin-Tub fabrication sequence, Fabrication process flow.
Layout Design and Design rules, Stick Diagram and Design rules-micron rules and Lambda rules. (definitions only).layout of CMOS Inverter, two input NAND and NOR gates.

Text Books:

1. Sung –Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits- Analysis & Design, McGraw-Hill, Third Ed., 2003
2. S.M. SZE, VLSI Technology, 2/e, Indian Edition, McGraw-Hill,2003
3. Wayne Wolf ,Modern VLSI design, Third Edition, Pearson Education,2002.

References:

1. Michael John Sebastian Smith, Application Specific Integrated Circuits, Pearson Education,2001.
2. Neil H.E. Weste, Kamran Eshraghian, Principles of CMOS VLSI Design- A Systems Perspective, Second Edition. Pearson Publication, 2005.
3. Jan M. Rabaey, Digital Integrated Circuits- A Design Perspective, Prentice Hall, Second Edition, 2005.
4. Razavi - Design of Analog CMOS Integrated Circuits,1e, McGraw Hill Education India Education, New Delhi, 2003.
5.

Course Contents and Lecture Schedule.

No	Topic	No. of. Lectures
Module 1: VLSI Design Methodologies. (11 Hrs)		
1.1	Introduction: Moore slaw .ASIC design, Full custom ASICs, Standard cell based ASICs, Gate array based ASICs,	**3**
1.2	SoCs, FPGA devices	**2**
1.3	ASIC and FPGA Design flows Top-Down and Bottom-Up design methodologies.	**3**
1.4	Logical and Physical design. Speed power and area considerations in VLSI design	**3**
Module 2:Static CMOS Logic Design (9 Hrs)		
2.1	**MOSFET Logic Design** - NMOS logic (Static analysis of Basic gates only)	**3**
2.2	CMOS logic, Static and transient analysis of CMOS inverter Switching power dissipation and delays	**3**
2.3	Realization logic functions in static CMOS logic, Pass transistor logic, and transmission gate logic (Static analysis only)	**3**
Module 3: Dynamic logic Design and Storage Cells (8 Hrs)		
3.1	Dynamic Logic Design-Pre charge- Evaluate logic, Domino Logic, NP domino logic.	**3**

3.2	**Read Only Memory**-4x4 MOS ROM Cell Arrays(OR,NOR,NAND)	**2**
3.3	**Random Access Memory** –SRAM-Six transistor CMOS SRAM cell, DRAM –Three transistor and One transistor Dynamic Memory Cell.	**3**
Module 4: Arithmetic circuits (5 Hrs)		
4.1	**Adders**- Static adder, Carry-Bypass adder, Linear Carry- Select adder, Square- root carry- select adder.	**3**
4.2	**Multipliers**-Array multiplier.	**2**
Module 5: MOSFET physical Design and Fabrication techniques (13 Hrs)		
5.1	**Material Preparation** (qualitative analysis only) Purification and Crystal growth (CZ process), wafer preparation.	**2**
5.2	**Thermal Oxidation-** Growth mechanisms, Dry and Wet oxidation. Diffusion and ion implantation techniques.	**3**
5.3	**Epitaxy :** Molecular beam epitaxy. **Lithography-** Photo lithographic sequence, Electron Beam Lithography, Etching and metal deposition techniques	**3**
5.4	**MOSFET Fabrication techniques**(*qualitative analysis only*) Twin-Tub fabrication sequence, Fabrication process flow.	**2**
5.5	**Layout Design and Design rules**, Stick Diagram and Design rules- micron rules and Lambda rules. Layout of CMOS Inverter, two input NAND and NOR gates,	**3**

Model Question Paper

A P J Abdul Kalam Technological University

Sixth Semester B Tech Degree Examination

Branch: Electronics and Communication Course:

ECT 304 VLSI CIRCUIT DESIGN

Time: 3 Hrs Max.

Marks: 100

PART A

(*Answer All Questions*)

1	What is Moore's law in VLSI design?	(3)
2	Differentiate between ASIC and FPGA.	(3)
3	Switching threshold voltage equation of CMOS inverter and explain each parameter	(3)
4	List the advantage of CMOS logic.	(3)
5	List the advantages of dynamic logic over static logic circuits.	(3)
6	Differentiate between volatile and non volatile memories.	(3)
7	Explain propagate delete and generate signals.	(3)
8	What are the different types of power dissipation in a CMOS inverter?	(3)
9	List the advantages of SiO2	(3)
10	Define lambda rules and micron rules.	(3)

PART B

(*Answer one question from each module. Each question carries 14 mark*.)

11(A)	What is FPGA? What are its applications? With block diagram explain its internal architecture?	(6)
11(B)	Explain ASIC design flow.	(8)
	OR	
12(A)	Compare different ASIC design methodologies.	(8)
12(A)	List the advantages of SOC	(6)
13(A)	Derive expression for the switching threshold of a CMOS inverter.	(7)
13(B)	What is meant by pass transistor logic? What are the differences in transmission characteristics of N MOS and P MOS transistors?	(7)
	OR	
14(A)	What are the different types of power dissipation in a CMOS inverter? Derive expression for the total power dissipation.	(8)
14(B)	Why PMOS transistor can pass only strong ones and NMOS can pass strong zeros.	(6)

15(A)	Draw the circuit diagram and explain the principle of operation of a CMOS based static RAM cell. Explain the read and write operations. What are the constraints on the sizes of transistors?	(7)
15(B)	Draw the circuit diagram and explain the principle of operation of a one transistor dynamic RAM cell. Explain the read, write and refresh operations	(7)
	OR	
16(A)	Explain the read and write operation of a three-transistor DRAM cell	(7)
16(B)	Explain the read and write operation of a six transistor CMOS SRAM cell.	(7)
	OR	
17(A)	With diagram illustrate the principle of operation of an array multiplier. Show the critical path. Estimate the delay of the multiplier.	(8)
17(B)	With block diagram illustrate the principle of operation of a square root carry select adder. Estimate the delay of an n bit adder	(6)
	OR	
18(A)	Draw circuit diagram of a full adder with not more than 28 transistors in standard CMOS logic	(8)
18(B)	Explain the working a 16-bit carry-by pass adder and write down the expression for worst-case delay.	(6)
19(A)	Illustrate with diagram the principle of crystal growth by Czochralzki method.	(7)
19(B)	What is photolithography? With diagram illustrate the steps involved in photolithography process.	(7)
	OR	
20(A)	Explain the principle of molecular beam epitaxy, with schematic diagram of an MBE system. What are its advantages and disadvantages?	(8)
20(B)	With schematic diagram and chemical reactions involved, illustrate wet and dry oxidation processes	(6)

MODEL ASSIGNMENT QUESTIONS

Module 1

1. How to choose between FPGA and ASIC ?
2. Describe ASIC in terms of Size, power and performance, IP protection and competitive Edge
3. Compare Gate-array design and Full-custom design?
4. What are the differences between CPLDs and CLBs
5. List some of the commonly used FPGA development board ?
6. Discuss the architecture of any one of the leading FPGA in industry ?

Module 2

1. Power and interconnect delay analysis of CMOS inverter?
2. Implement XOR function using pass transistor logic?
3. Derive V_{IL}, V_{IH},V_{OH}, and V_{OL} of depletion load inverter?
4. Design 8:1 MUX using transmission gate logic?
5. What are the advantages of NMOS over CMOS ?

Module 3

1. Explain the working of sense amplifiers in memory structures?
2. Design a voltage comparator in precharge-evaluate logic .
3. Discuss the cascading problem of P-E logic
4. Discuss the architecture of FLASH EPROM
5. Explain the working of FGMOS

Module 4

1. With diagram illustrate the principle of operation of an array multiplier. Show the critical path. Estimate the delay of the multiplier
2. Implement a 3x3 array multiplier?

Module 5

1. What is photolithography? With diagram illustrate the steps involved in photolithography process?
2. What is Deal Grove model of oxidation? What are linear and parabolic rate coefficients with reference to oxidation process?
3. Illustrate with diagram the principle of crystal growth by Czochralzki method
4. Explain DEAL-GROVE model of oxidation?
5. What are the requirements of a "clean-room" in VLSI fabrication